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VHDL DESIGNING IMPLEMENTATION OF NEW IMPROVED FULLY SYNCHRONOUS FREQUENCY METER

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Abstract: **Frequency is a basic parameter of electronics field. Meanwhile, it's a very important parameter. Stable clock is very important in high performance electronics system, determining the system performance directly. With the development of technology of electronics the frequency measurement system using higher clock, the frequency measurement technology has very nice development In despite of using all other advanced frequency measurement methods the positive and negative ±1 errors was a very important factor that stop frequency measurement precision improving although. The design expound the advantage and disadvantage of most digital frequency measurement methods Through analyzing the origin of the positive and negative ±1 error, got a new frequency measurement methods checking the measured and standard signal's phase if the phase is synchronous, then the counters start counting when the signal's phase is synchronous again the counter stopping working by phase in-phase to eliminate counting errors then getting the real frequency through calculating. By this way's guide, the design of complete digital frequency meter was successfully completed with using VHDL (Very High Speed Integrated Circuit Hard Design Language) hardware description language and simulated it right. According to all of Synchronous Digital Block diagram of the frequency measurement using VHDL the successful preparation of the design process, and in MAX+PLUS II software environment. The preparation of procedures for VHDL simulation obtained very good results.**

***Keywords*— XILINX ISE v 10.2, Max+ plus II, Model sim, complete in-phase, Spartan 3e**

I. INTRODUCTION

As digital circuit applications more widely, the traditional general-purpose digital integrated circuit chip has been difficult to meet the Department of Required system function, but with the increasing complexity of the system, the number of common integrated circuit was required burst Fried growth, so that the volume of the rapid expansion of the circuit board, the system reliability is not guaranteed. In addition, modern electronics Product life cycle is very short, one circuit may be modified within a very short time to meet new feature Seek, for it implies a universal integrated circuit redesign and re-wiring. The programmable logic device to overcome The above drawbacks, by programming it to a universal integrated circuit integrated onto a silicon wafer on a small, narrow doubled Volume of the circuit, and because traces short to reduce interference and improve the reliability of the system, and because VHDL Verilog language and easy to learn and use language accounted for, the design is quite flexible, greatly shortening the product Period. This design FPGA technology in more mature, more widely, the use of sophisticated FPGA Technology to achieve self-management project is not very mature fully synchronous digital frequency meter. This design has important research value.

II. PROBLEM FORMULATION: NEED AND SIGNIFICANCE OF PROPOSED RESEARCH WORK

After reading many research paper and literature survey and comparing various frequency measurement techniques we reach at following conclusion:

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- Direct frequency measurement method is convenient measurement readings directly in the relatively wide frequency within the range of high accuracy can be obtained. But the main disadvantage is the signal error of ± 1 digit Exist, it is difficult to achieve both low and high frequency, such as the accuracy of the measurement, the measurement accuracy is low.

- However, multi-cycle synchronous frequency measurement method is still not able to base Synchronizing signal and the measured signals and the three strobe signals, to produce a signal when the base quantization word ± 1The error is not eliminated.

- In the phase detection using multi-cycle Measurement of frequency synchronization method should take into account the relationship between the measured frequency difference signal frequency and signal frequency standards on the measurement accuracy affected. Certain standard frequency, frequency difference measured frequency and standard frequency is smaller, measuring the corresponding actual gate When asked will the longer; while the frequency difference is too large, considering the resolution of the phase detection circuit between the signal and the reference signal Phase coincidence pulse generation will no rules to follow. When not using the same two-phase pulse generated by coincidence Coincident with the separation rule offset detecting circuit detecting an error, can not achieve the highest measurement accuracy of this method Degrees.

III. Scheme Of Frequency Measurement To Improve Measurement Accuracy

To improve in the multi-cycle synchronous frequency measurement method, has eliminated the quantization error of the measured signal ± 1 word, but Quantization error is ± 1 standard frequency signal word has not yet been solved. Thus, the following more weeks in Synchronization frequency measurement method, based on the basic method to further improve the accuracy of the analysis.

3.1 Adopt amendments to the standard frequency signal count to improve measurement accuracy

A) Double counting frequency measurement: The multi-cycle synchronization method based on frequency measurement, to mention High frequency measurement accuracy. We were the standard frequency of rising and falling edges, respectively, as a counter count Pulse number N is equal to the final count value of the counter 2The arithmetic mean. In fact, this method is equivalent to no change in The case of variable operating frequency of the system allowed up to 2 times Frequency effects to 2 f_0 clock frequency counts, which will increase to twice the original measurement accuracy. For example F_0 directly 100MHz the tree as a standard frequency meter pulse, The maximum counting error of 10ns, which is equivalent to the double counting along Clock was 200MHz, counting error 5ns, while Maximum operating frequency of the system has not changed.

B) Digital phase frequency measurement: This idea has the double counting frequency measurement tired like place. One signal is called the phase shift as a reference, the other Phase one signal relative to the reference signal over move lag. Standard frequency after a phase shift rate get clk0, clk1, clk2, clk3, while clk1, clk2, clk3 relatively accordance with clk0 Second phase shift of 90 degrees, 180 degrees, 270 degrees. Four signals as a counter 1, 2 counter, counter 3,4 is a pulse counter, while T1 is an integer multiple of T_x and T1 as the start signal for all the counters Number, N = (N0 + N1 + N2 + N3) / 4. However, due to clk1, clk2, clk3 is f_0 divided by two, so these Methods for improving the frequency measurement precision and double counting frequency measurement method are equivalent, but more complex circuits. If Using FPGA internal resources to achieve accurate phase shift divide-case, its accuracy can be increased by 4 times. In short, the above two methods can improve the accuracy of frequency measurement in a certain extent. But still very difficult to suppress the quantization error signal is generated by a standard frequency ± 1 word. Multi-phase inspection cycle synchronization frequency measurement method using a relatively simple technique can ask the exact same gate when the number of standard frequency signals and the whole cycle counting frequency of the

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signal under test, thereby obtaining a high frequency measurement Accuracy.

3.2. Multi-phase inspection cycle synchronization frequency measurement method

Multi-phase inspection cycle synchronization frequency measurement principle of law: When the amount between the measured frequency and the frequency difference between the amounts of standard frequency, the relative phase of the two signals over time peek Period changes. Using specific phase detection circuit that detects the frequency of the measured signal phase coincidence information, and generates a corresponding phase coincidence pulses associated with the door open as the pulse count of the actual gate signal.

Scheduled gate time Tg

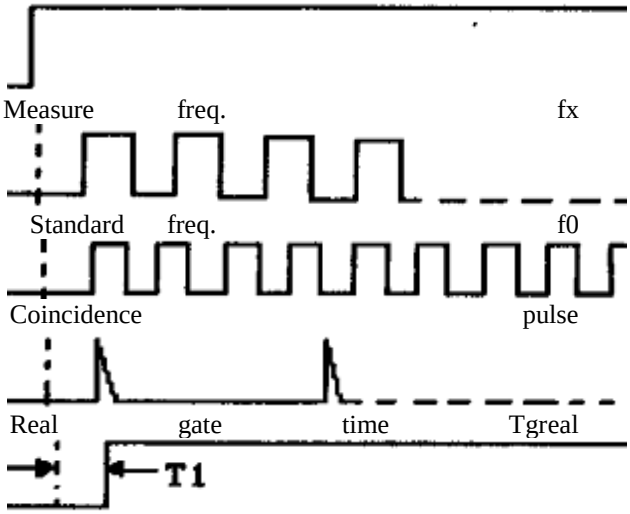

Fig 2.1 multi-cycle synchronization phase detection method of frequency measurement principle secluded

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f_x and f_0 were measured frequency signal and standard frequency signal, T_g is scheduled gate time (can be0.1s, 1s, 10s) given by the SCM system timing. After rising as high T_g pre-opening signal is given, Phase detection circuit began work, while f_x. And f_0 count does not really begin until then f_x. At the same time, and f_0 Rising or falling edge is reached, the phase detection circuit will produce a corresponding phase coincidence pulse, use it to open the true Positive gate count, two-way counter while f_x and f_0 are counting: After a predetermined gate when T_g after SCM pre-closing signal is given, but the count did not stop until the next pulse to coincide with the first phase To only two counters while closing, so too have two counters were measured frequency signal f. With standard Quasi-frequency signal f_0 integer number of cycles N_x and N_0. For f_0 to get to know are:

$$f_x = \frac{Nx}{N0} f_0$$

Frequency measured by this method, theoretically, only the measurement result obtained depends on the phase error detection circuit detecting a phase coincidence Measurement accuracy δ (such as the use 74SXX this series have high-speed devices can meet the detection accuracy in the timeline $\delta \leq 3$ns). However, this measurement method, in fact, a standard signal and the measured signal frequency, the frequency Rate difference was the size of the actual gate will affect the length of time too. Analysis shows that when the frequency difference is not, from the phase of the two signals overlap completely isolated by a regular change in a certain step. SCM gives pre- Open signal to the phase detection circuit detects the first phase coincidence then beat gate information and processes, and monolithic Machine gives a signal to the pre-closing phase detection circuit detects the subsequent first phase coincides information and close the gate tools exactly the same way, therefore, even though the phase coincidence detecting circuit for detecting a phase accuracy of J, but the gate opening Consistency both on and off the signal phase change process, this is the maximum offset by Susan Chan, measurement accuracy The higher the degree. However, the frequency difference is too small, two signal phase coincidence frequency is small, we can see from Figure 2.1, the actual gate time is Tgreal = Tg-T1 + T2, when T2 becomes too large will make the actual gate time is too long and thus too much Deviation from the preset gate time.

IV. Principle Of Fully Synchronous Digital Frequency Measurement

Fully synchronous frequency measurement: Direct method of measurement of frequency (M method for high freq. & L method for low freq) accuracy error depends not only on the reference count of counters date, also depends High and low frequencies,

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different frequencies are not the same precision, M method is relatively high in the high frequency accuracy, T method High accuracy of the low band. M/T rule in the accuracy of the entire plant to test the same band, the gate signal is measured signal An integer multiple number of cycles, i.e., synchronized with the signal, thus greatly reducing errors, but only with a mountain in the measured signal No synchronization without synchronization with the standard clock, so there is still a standard clock ± 1 counting error.

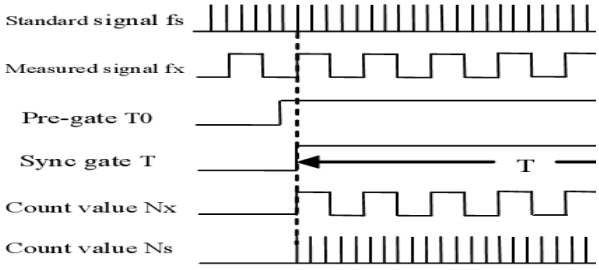

Figure3.1. Schematic diagram of equal precision measurement

When asked to set the actual gate T_0. In T_0 Within the time period measured as the number of signals N. Standard number of clock cycles As M_0. Standard clock frequency f_0, frequency measurement value of the measured signal:

$$f'_x = \frac{Nx}{M0} f_0 \qquad Eqn\ 1$$

When the actual gate T_x is an integer multiple of the signal cycle, N_x is accurate: while the standard clock The measured values of the errors exist $\Delta M0(|\Delta M0| \leq 1)$, i.e., the true value of the standard clock is counted to be the $M0 \pm \Delta M0$.This shows the true value of the measured signal frequency:

$$f_x = \frac{Nx}{(M0 + \Delta M0)} f_0 \qquad Eqn\ 2$$

Excluding the standard error of the clock the relative error of measurement is:

$$\sigma = \frac{|fx - f'x|}{fx} \times 100\% = \frac{|\Delta M0|}{M0} \leq \frac{1}{M0} = \frac{1}{T0f0} \qquad Eqn\ 3$$

From the above equation error and gate time and clock frequency, and when the gates standard clock frequency the higher the smaller the error. Since the standard clock frequency accuracy measurement taken with equal frequency method is relatively high (10MHZ), so ± 1 count error is relatively small. Raise the standard clock frequency can not be unlimited, and with the Frequency increases, product costs increase exponentially, does not make sense for production applications. Methods of measurement precision frequency measurements to achieve a fully synchronous digital frequency meter design. In the case of full synchronization, the gate signal is not synchronized with the signal, but also synchronized with the standard clock synchronization under achieve true. Its original Figure 3.1 shows the reason.

Let gate pulse synchronization when Δt_1 worse for her, difference Δt_2 pulse synchronization closed gates. The maximum error of pulse synchronous detection Δt, there are: $\Delta t_1 \leq \Delta t$, $\Delta t_2 \leq \Delta t$ excluding the standard clock error, the real Inter gate with the standard clock synchronization, actual gate time is T_0 '. The signal count value N_x. Standard clock count M_0 value is, the frequency measurement of the signal is '"

$$f'_0 = \frac{Nx}{T0} = \frac{Nx}{M0} f_0 \qquad Eqn\ 4$$

The real value of the signal frequency can be expressed as:

$$f_x = \frac{Nx}{T0 + \Delta t1 + \Delta t2} f_0 \qquad Eqn\ 5$$

Relative frequency measurement error is:

$$\sigma = \frac{|fx - f'x|}{fx} \times 100\% = \frac{|\Delta t1 + \Delta t2|}{T0} \leq \frac{2|\Delta t|}{T0} \qquad Eqn\ 6$$

From the above equation, the error is only accurate pulse detection circuit related.

V. Design Implementation Of New Improved Synchronous Frequency Meter

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Design schematic mainly consists of the following parts: Pulse synchronous detection circuit, two counters, two latches, controllers, multipliers, dividers, decoding circuit and other components.
Works as follows: the measured frequency and standard clock pulses are sent to the synchronous detection circuit with two Counter when the synchronization detection circuit detects the pulse frequency of the standard clock to the measured phase synchronization, the synchronization pulse Issue a sync signal detection circuit, two counter begin counting again when the pulse synchronous detection circuit detects When the sync signal, also issued a sync signal, the counter stop counting. Taking into account the value of the counter to lock latch Memory, timing obtained from the multiplier latches the count value of the measured frequency and the standard clock frequency multiplication Count, then the count value obtained by the multiplier with the standard operation of the clock divider to the multiplier If the count of the dividend, the value of the standard clock divisor, the result is the frequency of the signal computation proceeds, then After two decimal conversion and then become BCD code, give digital display. When the design standards adopted 10MHzBell, because of the multiplier is 27 binary inputs, equivalent to 9 I/O hexadecimal numbers, while the standard clock 10MHz, therefore multiplied by 10^n to obtain a decimal count value measured frequency. The following describes the various modules. Function of the circuit and the implementation process.

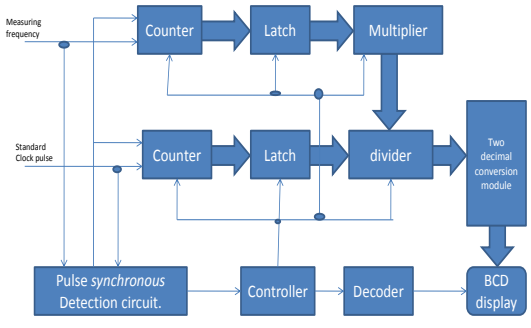

Figure: block diagram of the synchronous frequency meter

Figure 5.1: Block Diagram of synchronous Frequency Meter

VI. Stimulation Result & Synthesis Report

The simulation can be seen from the diagram: 124 × 10^7 ÷ 93 = 13333333, since using a 10MHz crystal, so there is a decimal point final results should be displayed 1333333.3Hz. Figure 5.1 from the simulation knowledge, in the second decimal place on effective digital tube, there was no remaining bits Effect. The simulation results are consistent with the expected results. After compiled stimulation is show in figure 5.2.

In Figure 5.1 is obtained through local amplification simulation map, you can more clearly see the digital control Display case: 1001111 display digital 3, 0000110 display digital 1, 0111111 display digital 0, and also There are instructions decimal point in the penultimate position, indicating that the last show on the digital control is: 01333333.3.This is exactly the same with the theoretical calculations. You can clearly see the two sets of data, one of which is: 124 × 10^7 ÷93 = 13333333; another set of data is: 13 × 101 ÷69 = 1884057. This fully explains who the accuracy of the design. Since the basic design criteria adopted 10MHz of Reference frequency, so the frequency of the signal can not be too high. If more than 100MHz frequencies through the system Measure will make the measurement error increases, while the internal counter FPGA devices can not meet the requirements. But this system can be extended with a circuit to realize the measurement of higher frequency.

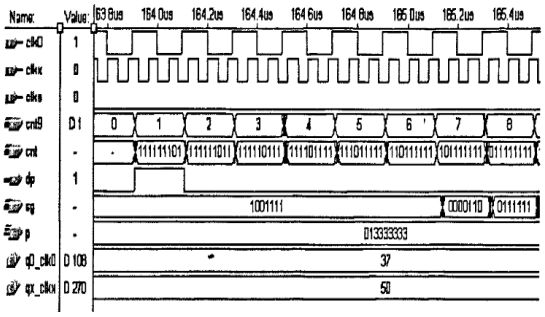

Figure 6.1: overall simulations Figure

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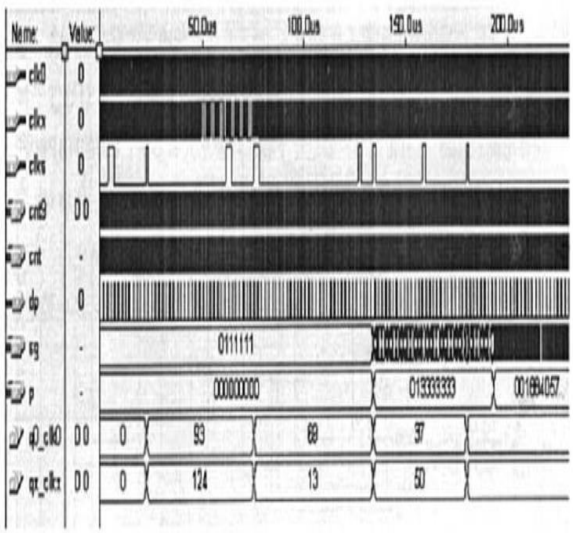

FIGURE 6.2: COMPLETE STIMULATION AFTER COMPILED

A) Design Information

- The controller was synthesized on FPGA XC3s 200 using Xilinx ISE 9.2i.
- Device utilization summary: Target Device: xc3s100e, Target Package: tq144, Target Speed : -5

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	73	1,920	3%	
Number of 4 input LUTs	168	1,920	8%	
Logic Distribution				
Number of occupied Slices	101	960	10%	
Number of Slices containing only related logic	101	101	100%	
Number of Slices containing unrelated logic	0	101	0%	
Total Number of 4 input LUTs	182	1,920	9%	
Number used as logic	168			
Number of bonded IOBs	62	108	57%	
IOB Flip Flops	40			
IOB Latches	9			
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	2,392			
Additional JTAG gate count for IOBs	2,976			

VII. CONCLUSIONS & FUTURE SCOPE

All-purpose synchronous digital frequency meter is self highest precision frequency meter. In the high-speed clock can be seen everywhere in modern power Subsystem has a very wide range of research value. To some extent that it is at the expense of time in exchange for accurate Degree, but under normal circumstances frequency meter times is not high, and because the electronic systems on the system clock Accuracy requirements are high, and therefore the whole or synchronous digital frequency meter has a broad application space. By The whole design of synchronous digital frequency meter, we can get the following conclusions:

- A fully synchronous frequency measurement principle eliminates ± 1 count errors and improves frequency measurement accuracy.
- The fully synchronous digital frequency meter design on the FPGA chip, constitute a typical SOC system, Reduce the size of the circuit board and shorten the design cycle has very important significance.
- The simulation of the whole synchronous digital frequency meter, and get a good result, which is the hardware design and provide a good test according to design.
- The design of the product should be converted into further study, and the need to design a power supply circuit Measured signal waveform shaping, amplification circuit and design standards and stable time base signal circuits.
- For measuring the frequency of the instrument function is generally better than more, so that we can in this design Basis, you can add test week, the measured phase

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difference and the Pc machine communication features that make it more functional side to development

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